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EXAMINER	
BADER, ROBERT N.	
ART UNIT	PAPER NUMBER
2628	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,376	SATOH, JIN	
	Examiner	Art Unit	
	ROBERT BADER	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :9/22/06, 10/17/06, 9/28/07, 1/30/09.

DETAILED ACTION

1. This Office Action is in response to the Applicants' communication filed on 1/30/09. In virtue of this communication, claims 1-19 are currently presented in the instant application.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claim 16 is rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. A process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing. The method claims are not patent eligible processes under § 101 and are rejected as being directed to a non-statutory subject matter.

Regarding claim 16 the claim limitations fail to tie the process to another statutory class, and therefore could be completed as a series of mental and human implemented steps.

In keeping with the requirement that a process claim should be tied to a machine or apparatus, the following operations procedure is set forth:

"Identifying the apparatus" requires that the process claim explicitly recite the particular machine or apparatus, or recite a step that inherently involves the use of a particular machine or apparatus. The step requires a particular machine or apparatus

such that the step cannot be performed mentally or manually in a manner that reasonably accomplishes the intended purpose of the recited invention, as claimed, without the use of a structure.

4. Claims 18 and 19 are rejected under 35 U.S.C. 101 because the claimed "computer program product" invention is directed to non-statutory subject matter. A program is not a process, machine, manufacture, or composition of matter. Claims 18 and 19 are drawn to functional descriptive material not claimed as residing on a computer readable medium. See MPEP 2106.IV.B.1 (a) (Functional Descriptive Material).

Claims 18 and 19, while defining a computer program product, does not define a "computer-readable medium" and is thus non–statutory for that reason. A computer program product can range from paper on which the program is written, to a program simply contemplated and memorized by a person.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "a unit throughput in which the area writer writes the subareas into the memory at a time" is indefinite because it is unclear what "at a time" refers to. It

appears to the examiner that the intent is to limit the throughput unit to equate to the subarea unit size. For purposes of applying prior art, the claim language will be considered to read “a unit throughput in which the area writer writes the subareas into memory one subarea at a time.”

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication 2004/0212619 A1 (hereinafter **Saito**).

Regarding all claims, it is noted that applicant uses the terms "unit area" (claims) and “stamp” (specification) to refer to the concept of a first level unit of division, which Saito terms "chunk". Applicant's terms "subarea" (claims) and "quad" (specification) are likewise equivalent to the second level unit of division, which Saito terms “stamp”.

Regarding claim 1, the limitation “a rasterizing unit which divides a unit figure into a plurality of unit areas on the screen coordinate system and outputs the unit areas” is taught by Saito (paragraphs 63-64, “The rasterizer 10 performs the processing of expanding a polygon on an image memory on a pixel-by-pixel basis. Pixel-by-pixel colors are determined by interpolating colors given to respective vertexes by a method

called smooth shading. The rasterizer 10 outputs pixel-by-pixel data as a rasterization result to the chunk merge unit 100. The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data.")

The limitation “an area divider which divides each of the unit areas output from the rasterizing unit into a plurality of subareas” is taught by Saito (paragraph 77, “FIG. 10 is a block diagram showing another configuration example of the chunk merge unit 100 according to this embodiment in detail. In this example, a block shown in Fig. 10 is provided for every pixel. Accordingly, in this embodiment, the number of blocks shown in FIG. 10 must be the same as the number of pixels in a stamp. Since 2x2=4 pixels constitutes one stamp in this embodiment, four blocks shown in FIG. 10 are needed for one stamp." Although Saito does not explicitly outline the relationship between chunks, stamps, pixels, and the hardware components of the disclosed system, Fig. 10 shows that the chunk merge unit has an equal number of blocks (one block corresponds to one pixel) as there are pixels in a stamp, meaning that the chunk merge unit processes a single stamp at a time.)

The limitation “an area discarder which discards as necessary a subarea obtained by the division by the area divider according to a predetermined rule" is taught by Saito (paragraph 80-81, “The chunk flush controller 132 determines whether pixel or stamp data inputted from the rasterizer 10 and pixel of stamp data in the chunk flush controller 132 conflict with each other. Alternatively, the chunk flush controller 132 determines which data is to be left according to their pixel depths. When both data conflict with each other, the chunk flush controller 132 transmits chunk data in the chunk

data buffer 110 at this point in time to the pixel processor 20, defines a new chunk, and write the pixel data inputted from the rasterizer 10 in the new chunk. Moreover, if the data to be left can be determined based on the pixel depths and the like, the chunk merge unit 100 determines whether the pixel data inputted from the rasterizer 10 is abandoned or the pixel data inputted from the rasterizer 10 is overwritten in the chunk data buffer 110.")

The limitation "an area writer which writes a subarea that survived the discarding process by the area discarder into a memory" is taught by Saito (paragraph 64, "The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data. Data resulted from the merger is outputted to the chunk data buffer 110.")

Regarding claim 2, the limitation "wherein the area writer re-merges subareas that survived the discarding process and writes merged areas obtained by re-merges in the memory" is taught by Saito (paragraphs 98-100, "FIG. 16 is a flowchart for explaining stamp-by-stamp merging processing such as shown in FIG. 14 and FIG. 15. The merging processing shown in FIG. 16 is different from the merging processing shown in FIG. 13 in step S220. Namely, in the merging processing in FIG. 16, after step S120, it is determined whether a chunk in the same position exists and a conflict occurs to any one of all pixels in a stamp constituting the chunk (step S220). When no conflict occurs (step S220: No), the stamp is written as pixel data into the exiting chunk (step S170). On the other hand, if a conflict occurs to any one of pixels in the stamp (step S220: Yes), the chunk is flushed (step S150) and cleared (step S160). Namely, all

of four pixels in a stamp which are processed at the same time are written into the existing chunk data buffer 110 or written into a newly generated chunk.")

Regarding claim 3, the limitation "wherein each of the merged areas has the same size as the unit area" is taught by Saito (Figures 3, 11, 12, 14, 15, 17, 18 all show pre-merge and post-merge chunks being the same size.)

Regarding claim 4, the limitation "wherein the size of the subarea corresponds to a unit throughput in which the area writer writes the subareas into the memory one subarea at a time" is taught by Saito (paragraph 77, as quoted above. The number of blocks in the chunk merge unit is equivalent to the number of pixels in a stamp, meaning each unit of throughput from the chunk merge unit will correspond to the stamp size.)

Regarding claim 5, the limitation "wherein, of the subareas that survived the discarding process by the area discarder, the area writer merges subareas derived from unit areas having the same coordinates in the screen coordinate system before the division" is taught by Saito (paragraph 146, "As described above, in the example in FIG. 24, when plural existing stamps exist in the same position, a stamp in which no conflict occurs is found from the existing stamps.")

Regarding claim 6, the limitation "wherein the area writer refers to information indicating the relative position of a subarea in the unit area to which the subarea belonged before the division and writes the subarea in an address in the memory corresponding to the information" is taught by Saito (paragraph 120, "FIG. 21 is a flowchart explaining the processing contents of the store/read mechanism shown in

FIG. 20. As shown in FIG. 21, a stamp position is first acquired (step S300). A chunk position is then acquired (step S310)." Stamp positions are stored separate from chunk positions, and must inherently be relative, otherwise there would be a determination step required (deriving chunk from stamp position) or excessive redundancy (stamp position would contain chunk position, which is already stored elsewhere). Paragraph 116, "The chunk data d is 8x8=64 pixel information. Namely, the chunk data d is concrete pixel data on the entry." In order to write the stamps to the correct position in the chunk data, d, the relative position of the stamp must be utilized (i.e. the stamp in the upper left will correspond to a different area of the chunk data, d, than the stamp in the lower right). It should be noted that although Saito does teach the use of relative stamp positions in merging and writing data, **Saito does not teach the process of stamp/quad/subarea relocation** within a given tile/stamp/unit area as described by applicant, though not recited in the claims.)

Regarding claim 7, the limitation "wherein the unit area is a rectangular area, the rasterizing unit divides a rendering area so that each of the plurality of unit areas includes a pixel group, the pixel number in the vertical direction and the pixel number in the horizontal direction of a pixel group in a given unit area being identical with the corresponding numbers of a pixel group in another unit area" is taught by Saito (paragraph 61, "In the example in FIG. 3, one chunk is composed of 8x8=64 pixels. This chunk is a fragment in this embodiment. By using the concept of the chunk, it is guaranteed that pixels which are continuously thrown in are not in the same position, and the chunk is processed by a pixel processor." While not explicitly stated by Saito, it

is inherent that all chunks must be of equivalent size, because there is no consideration given to determining the size of any given chunk in the disclosure. If chunks were to vary in size, the invention would become inoperable. While Saito also fails to explicitly state that chunks are rectangular, all provided examples (in both figures and text) are rectangular, making this an implicit feature of Saito's disclosure.)

The limitation "the area divider divides the unit area including the pixel group into a plurality of subareas each including a small pixel group, the pixel number in the vertical direction and the pixel number in the horizontal direction of a pixel group in a given subarea being identical with the corresponding numbers of a pixel group in another subarea" is taught by Saito (paragraph 77, "Accordingly, in this embodiment, the number of blocks shown in FIG. 10 must be the same as the number of pixels in a stamp. Since 2x2=4 pixels constitutes one stamp in this embodiment, four blocks shown in FIG. 10 are needed for one stamp." Similar to the logic presented in the previous paragraph, while not explicitly stated that stamps must be of equivalent size, it is inherent to the invention, because there is no consideration given to determining the size of any given stamp. If stamps were to vary in size, the invention would become inoperable.")

Regarding claim 8, the limitation "wherein, of the plurality of subareas obtained by the division by the area divider, the area discarder discards a subarea that does not include any valid pixels" Is taught by Saito (paragraph 91, "The processing from step S130 to step S170 is performed by the chunk flush controller 132 of the chunk merge unit 100. Condition determination as to whether a conflict occurs or not is performed by

the value comparison circuit 136 and the AND circuit 138." Paragraph 74, "Coverage and pixel parameters are data inputted from the rasterizer 10. The coverage is information indicating whether the pixel parameters are valid or invalid. That is, the coverage is information indicating whether it is inside or outside the triangle." As shown in Figure 10, the coverage information is used to determine if a pixel is valid (an input to AND 138), which is used to determine if a stamp is valid. A stamp without any valid data will not be written, as shown in Figure 15, where some 2x2 stamps contain 1 or more invalid pixels (empty circles), but no stamps contain a full 4 invalid pixels.)

Regarding claim 9, the limitation "wherein, of the subareas that survived the discarding process by the area discarder, the area writer re-merges subareas which do not include valid pixels at identical coordinates in the screen coordinate system and writes merged areas obtained by re-merge in memory" is taught by Saito (paragraphs 89-90, "Then, the chunk merge unit 100 acquires pixels in a stamp (step S120). Subsequently, the chunk merge unit 100 determines whether two chunks to be merged are in the same position and a conflict occurs to any of all pixels in respective stamps (step S130). When no conflict occurs to any pixel (step S130: No), pixel data is additionally written into the existing chunk (step S170). On the other hand, if a conflict occurs to any pixel (step S130: Yes), only pixels which do not conflict are additionally written into the existing chunk and pixel data which has been written is deleted from write data (step S140). Subsequently, after flushing the chunk (step S150), the chunk merge unit 100 clears the chunk (step S160). Then, the chunk merge unit 100 writes the remaining pixel data into this new chunk.")

Regarding claim 10, the limitation "wherein, of the subareas that survived the discarding process by the area discarder, the area writer merges subareas derived from unit areas having the same coordinates in the screen coordinate system before the division" is taught by Saito (paragraph 86, "On the other hand, in the example in FIG. 12, pixel data in the chunk 1 stored in the chunk data buffer 110 and pixel data in the chunk 2 inputted from the rasterizer 10 overlap each other. Namely, these pixel data exists at the same X coordinate and Y coordinate. Therefore, new pixels of the chunk 2 are added only to pixels, in which no data exists, of the chunk 1, and the remaining pixels of the chunk 2 are generated as pixels of the new chunk 2.")

Regarding claim 11, the limitation "wherein the area writer refers to information indicating the relative position of a subarea in the unit area to which the subarea belonged before the division so as to write the subarea in an address in memory corresponding to the information" is taught by Saito (paragraph 120, "FIG. 21 is a flowchart explaining the processing contents of the store/read mechanism shown in FIG. 20. As shown in FIG. 21, a stamp position is first acquired (step S300). A chunk position is then acquired (step S310)." Stamp positions are stored separate from chunk positions, and must inherently be relative, otherwise there would be a determination step required (deriving chunk from stamp position) or excessive redundancy (stamp position would contain chunk position, which is already stored elsewhere). Paragraph 116, "The chunk data d is 8x8=64 pixel information. Namely, the chunk data d is concrete pixel data on the entry." In order to write the stamps to the correct position in the chunk data, d, the relative position of the stamp must be utilized (i.e. the stamp in

the upper left will correspond to a different area of the chunk data, d, than the stamp in the lower right).)

Regarding claim 12, the limitation “wherein the area writer comprises a memory access unit which writes pixels included in the subarea into memory in parallel” is taught by Saito (paragraph 66, “The image rendering device shown in FIG. 4 has the most basic configuration, and one chunk data buffer 110 and one pixel processor 20 are provided for one chunk merge unit 100. It is possible to simultaneously store one or more pieces of chunk data in the chunk data buffer 110.”)

Regarding claim 13, the limitation “rasterizing by dividing a unit figure into a plurality of unit areas on the screen coordinate system and outputting the unit area” is taught by Saito (paragraphs 63-64, “The rasterizer 10 performs the processing of expanding a polygon on an image memory on a pixel-by-pixel basis. Pixel-by-pixel colors are determined by interpolating colors given to respective vertexes by a method called smooth shading. The rasterizer 10 outputs pixel-by-pixel data as a rasterization result to the chunk merge unit 100. The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data.")

The limitation “dividing each of the unit areas output from the rasterizing into a plurality of subareas” is taught by Saito (paragraph 77, “FIG. 10 is a block diagram showing another configuration example of the chunk merge unit 100 according to this embodiment in detail. In this example, a block shown in Fig. 10 is provided for every pixel. Accordingly, in this embodiment, the number of blocks shown in FIG. 10 must be

the same as the number of pixels in a stamp. Since 2x2=4 pixels constitutes one stamp in this embodiment, four blocks shown in FIG. 10 are needed for one stamp.")

The limitation “discarding as necessary a subarea obtained by dividing the unit area according to a predetermined rule" is taught by Saito (paragraph 80-81, “The chunk flush controller 132 determines whether pixel or stamp data inputted from the rasterizer 10 and pixel of stamp data in the chunk flush controller 132 conflict with each other. Alternatively, the chunk flush controller 132 determines which data is to be left according to their pixel depths. When both data conflict with each other, the chunk flush controller 132 transmits chunk data in the chunk data buffer 110 at this point in time to the pixel processor 20, defines a new chunk, and write the pixel data inputted from the rasterizer 10 in the new chunk. Moreover, if the data to be left can be determined based on the pixel depths and the like, the chunk merge unit 100 determines whether the pixel data inputted from the rasterizer 10 is abandoned or the pixel data inputted from the rasterizer 10 is overwritten in the chunk data buffer 110.”)

The limitation “writing a subarea that survived the discarding into a memory” is taught by Saito (paragraph 64, “The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data. Data resulted from the merger is outputted to the chunk data buffer 110.”)

Regarding claim 14, the limitations are similar to those treated in the above rejection(s) and are met by the references as discussed in claim 7 above.

Regarding claim 15, the limitations are similar to those treated in the above rejection(s) and are met by the references as discussed in claim 8 above.

Regarding claim 16, the limitation “dividing a unit figure into a plurality of unit areas on the screen coordinate system and outputting the unit areas” is taught by Saito (paragraphs 63-64, “The rasterizer 10 performs the processing of expanding a polygon on an image memory on a pixel-by-pixel basis. Pixel-by-pixel colors are determined by interpolating colors given to respective vertexes by a method called smooth shading. The rasterizer 10 outputs pixel-by-pixel data as a rasterization result to the chunk merge unit 100. The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data.")

The limitation “generating merged areas by retrieving, from a plurality of subareas constituting each of the unit areas output from the dividing, subareas that include valid pixels” is taught by Saito (paragraph 85, “In the merging processing shown in FIG. 11 and FIG. 12, whether pixels in respective chunks conflict with each other is determined on a pixel-by-pixel basis and the chunks are merged on a pixel-by-pixel basis.”)

Regarding claim 17, the limitation “dividing a unit figure into a plurality of unit areas on the screen coordinate system and outputting the unit areas” is taught by Saito (paragraphs 63-64, “The rasterizer 10 performs the processing of expanding a polygon on an image memory on a pixel-by-pixel basis. Pixel-by-pixel colors are determined by interpolating colors given to respective vertexes by a method called smooth shading. The rasterizer 10 outputs pixel-by-pixel data as a rasterization result to the chunk merge unit 100. The chunk merge unit 100 converts the pixel-by-pixel data into chunk-by-chunk data and performs a merger of data.")

The limitation "writing subareas, of a plurality of subareas constituting each of the unit areas output from the dividing, that include valid pixels into a memory" is taught by Saito (paragraph 91, "The processing from step S130 to step S170 is performed by the chunk flush controller 132 of the chunk merge unit 100. Condition determination as to whether a conflict occurs or not is performed by the value comparison circuit 136 and the AND circuit 138." Paragraph 74, "Coverage and pixel parameters are data inputted from the rasterizer 10. The coverage is information indicating whether the pixel parameters are valid or invalid. That is, the coverage is information indicating whether it is inside or outside the triangle." As shown in Figure 10, the coverage information is used to determine if a pixel is valid (an input to AND 138), which is used to determine if a stamp is valid. A stamp without any valid data will not be written, as shown in Figure 15, where some 2x2 stamps contain 1 or more invalid pixels (empty circles), but no stamps contain a full 4 invalid pixels.)

The limitation "writing subareas, … into a memory in parallel" is taught by Saito (paragraph 66, "The image rendering device shown in FIG. 4 has the most basic configuration, and one chunk data buffer 110 and one pixel processor 20 are provided for one chunk merge unit 100. It is possible to simultaneously store one or more pieces of chunk data in the chunk data buffer 110.")

Regarding claim 18, the limitations are similar to those treated in the above rejection(s) and are met by the references as discussed in claim 16 above.

Regarding claim 19, the limitations are similar to those treated in the above rejection(s) and are met by the references as discussed in claim 17 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT BADER whose telephone number is (571)270-3335. The examiner can normally be reached on M-T 9am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ROBERT BADER
Examiner
Art Unit 2628

/Ulka Chauhan/

Supervisory Patent Examiner, Art Unit 2628